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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/888,463	06/25/2001	Hermanus Leonardus Peek	NL 000359	8680
27082	7590	10/07/2003	EXAMINER	
DORSEY & WHITNEY LLP 1001 PENNSYLVANIA AVENUE, N.W. SUITE 400 SOUTH WASHINGTON, DC 20004				FOURSON III, GEORGE R
ART UNIT		PAPER NUMBER		
		2823		

DATE MAILED: 10/07/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

**UNITED STATES DEPARTMENT OF COMMERCE****U.S. Patent and Trademark Office**

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09/888 463

APPLICATION NO./ CONTROL NO.	FILING DATE	FIRST NAMED INVENTOR / PATENT IN REEXAMINATION	ATTORNEY DOCKET NO. 96
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EXAMINER

ART UNIT PAPER

18

DATE MAILED:

**Please find below and/or attached an Office communication concerning this application or proceeding.**

**Commissioner for Patents**

In response to applicant's telephone inquiry regarding the last Office action, the following corrective action is taken. The period for reply of 1 MONTHS set in said Office Action is restarted to begin with the mailing date of this letter.

See attached corrected copy of the last Office action which now indicates that the rejection is based on Hawkins et al 5,563,801.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group Receptionist whose telephone number is (703) 308-0956. See MPEP 203.08.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to examiner George Fourson whose telephone number is (703) 308-2544. The examiner can normally be reached on Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri, can be reached on (703) 306-2794. The fax number for this group is (703)308-7722 (or extensions 7724, 3431 or 3432) for regular communications and (703)308-7382 for after final communications.

George Fourson  
Primary Examiner  
Art Unit 2823

GFourson  
October 1, 2003



George Fourson  
Primary Examiner  
Art Unit: 2823

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 5/7/03 has been entered.

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claims 1-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hawkins et al '801 in combination with applicant's admitted prior art.

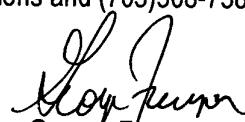
Applicant admits the process of forming strip-shaped semiconductor regions in a first direction by implantation through an oxide layer followed by removal of the oxide layer and formation of a gate dielectric upon which is formed strip-shaped gate electrodes running perpendicular to the first direction to have been known prior to applicant's invention. The admitted prior art process does not include implantation through the gate dielectric material upon which is formed a gate.

Hawkins et al is applied as stated in the rejections under U.S.C. § 102 and 35 U.S.C. § 35 U.S.C. § 103(a) in the office action mailed 4/22/03 as disclosing formation of electrodes on a nitride oxide gate dielectric through which implantation has been performed thus providing motivation to implant through a retained nitride/oxide gate dielectric material as opposed to the sacrificial oxide material of the admitted prior art process.

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